



# SHIVAJI UNIVERSITY, KOLHAPUR

## Department of Technology

Tel: 0231-2605970 E-mail: director.tech@unishivaji.ac.

A  
Accredited By NAAC

---

### INVITATION FOR QUOTATION

---

TEQIP-III/2019/dtsk/Shopping/67

26-Feb-2019

To,

**Sub: Invitation for Quotations for supply of Goods**

Dear Sir,

1. You are invited to submit your most competitive quotation for the following goods with item wise detailed specifications given at Annexure I,

Sr. No	Brief Description	Quantity	Delivery Period(In days)	Place of Delivery	Installation Requirement (if any)
1	MICROWIND 3.5	1	30	Department of Technology Shivaji University kolhapur	yes

2. Government of India has received a credit from the International Development Association (IDA) towards the cost of the **Technical Education Quality Improvement Programme[TEQIP]-Phase III** Project and intends to apply part of the proceeds of this credit to eligible payments under the contract for which this invitation for quotations is issued.
3. Quotation,

3.1 The contract shall be for the full quantity as described above.

3.2 Corrections, if any, shall be made by crossing out, initialing, dating and re writing.

3.3 All duties and other levies payable by the supplier under the contract shall be included in the unit price.

3.4 Applicable taxes shall be quoted separately for all items.

3.5 The prices quoted by the bidder shall be fixed for the duration of the contract and shall not be subject to adjustment on any account.

3.6 The Prices should be quoted in Indian Rupees only.

4. Each bidder shall submit only one quotation.

5. Quotation shall remain valid for a period not less than **45** days after the last date of quotation submission.

6. Evaluation of Quotations,

The Purchaser will evaluate and compare the quotations determined to be substantially responsive i.e. which

6.1 are properly signed ; and

6.2 confirm to the terms and conditions, and specifications.

7. The Quotations would be evaluated for all items together.

8. Award of contract:

The Purchaser will award the contract to the bidder whose quotation has been determined to be substantially responsive and who has offered the lowest evaluated quotation price.

8.1 Notwithstanding the above, the Purchaser reserves the right to accept or reject any quotations and to cancel the bidding process and reject all quotations at any time prior to the award of contract.

8.2 The bidder whose bid is accepted will be notified of the award of contract by the Purchaser prior to expiration of the quotation validity period. The terms of the accepted offer shall be incorporated in the purchase order.

9. Payment shall be made in Indian Rupees as follows:

**Delivery and Installation - 90% of total cost**

**Satisfactory Acceptance - 10% of total cost**

10. All supplied items are under warranty of **12** months from the date of successful acceptance of items.
11. You are requested to provide your offer latest by **18:00** hours on **23-May-2019**.
12. Detailed specifications of the items are at Annexure I.
13. Training Clause (if any) **yes**
14. Testing/Installation Clause (if any) **yes**
15. Information brochures/ Product catalogue, if any must be accompanied with the quotation clearly indicating the model quoted for.
16. Sealed quotation to be submitted/ delivered at the address mentioned below,
17. We look forward to receiving your quotation and thank you for your interest in this project.

(Authorized Signatory)  
Name & Designation

### Annexure I

Sr. No	Item Name	Specifications
1	MICROWIND 3.5	<ul style="list-style-type: none"> <li>➤ Library based schematic editor with facility to create symbols.</li> <li>➤ Library of various digital models like gates, registers, 74xx series devices, etc.</li> <li>➤ Both conventional pattern-based logic simulation and intuitive on-screen mouse-driven simulation.</li> <li>➤ Supports hierarchical logic design with built-in extractor which generates a SPICE netlist from the schematic diagram (compatible with pSpice and WinSpice)</li> </ul>

		<ul style="list-style-type: none"><li>➤ Generation of Verilog description of the schematic for layout generation.</li><li>➤ MOS level schematic support.</li><li>➤ Fault analysis tool at the gate level of digital circuits. Faults: Stuck-1, stuck-at-0.</li><li>➤ Immediate access to symbol properties of models like delay, fanout.</li><li>➤ Models and assembly support for 8051 and PIC 16F84 with facility to simulate with external circuits.</li><li>➤ Sub-micron, deep-submicron, nanoscale technology support.</li><li>➤ Facility to list delays of path and support critical path analysis.</li><li>➤ User-friendly advance CMOS layout design and simulation tool with FinFet technology support.</li><li>➤ FinFet device support with 2D cross section, 3D visualization, and layout construction.</li><li>➤ Design-error-free cell library (contacts, vias, MOS devices, etc.)</li><li>➤ Facility to convert CMOS layout in schematic, compatible with DSCH.</li><li>➤ Advanced macro generator: MOS, capa, matrix, ROM, pads, path, etc..)</li><li>➤ Ease in navigation for very large designs.</li><li>➤ Incredible translator from logic expression into compact design-error free layout</li><li>➤ Powerful automatic compiler from Verilog circuit into layout.</li><li>➤ Verilog compiler with various automatic routing methods like standard and compact.</li><li>➤ On-line design rule checker: width, spacing, overlap, extension rule verification</li><li>➤ Built-in extractor which generates a SPICE netlist from layout</li></ul>
--	--	---

		<ul style="list-style-type: none"><li>➤ Extraction of all MOS width and length</li><li>➤ Parasitic capacitance, crosstalk and resistance extracted for all electrical nodes</li><li>➤ Import/Export CIF layout from 3rd party layout tools</li><li>➤ Lock &amp; unlock layers to protect some part of the design from any changes</li><li>➤ Enhanced editing commands and layout control</li><li>➤ Built-in SPICE-like analog simulator features fast time-domain, voltage and current estimation, with very intuitive post processing: frequency estimation, delay estimation. (No external SPICE/ analog simulator.)</li><li>➤ To be supplied with WinSpice Simulator, for third party simulation of examples.</li><li>➤ Supports LEVEL1, LEVEL3 and BSIM4 models for all technologies from 1.2<math>\mu</math>m down to 14nm FinFET.</li><li>➤ MOS characteristic viewer, with access to main model parameter</li><li>➤ Real-case measurement data-base in 0.7,0.35, 0.25 and 0.18<math>\mu</math>m for comparison with models</li><li>➤ The ability to label nodes allows intuitive control of the simulation (supply, clock, pulse, PWL, sinus, maths)</li><li>➤ Time-domain voltage and current waveforms available at the press of one single icon</li><li>➤ DC/AC characteristics, signal frequency vs. time, eye diagrams</li><li>➤ Min/Typ/Max analog simulation</li><li>➤ Convenient Monte-carlo simulation</li><li>➤ Powerful fast-Fourier Transform to support radio-frequency circuit simulation</li><li>➤ On screen Power estimation</li><li>➤ Storage of simulation results in external CSV file format.</li></ul>
--	--	--

		<ul style="list-style-type: none"><li>➤ Sophisticated parametric simulation to investigate the effect of several key parameters on the circuit performances: R,L,C, temperature, supply voltage, etc.</li><li>➤ Huge device simulation model library</li><li>➤ Inbuilt interconnect analyzer to compute field between ground planes and conductor</li><li>➤ MOS characteristics viewer with the model parameters and visualization of their effects on <math>I_d/V_d</math>, <math>I_d/V_g</math>, <math>I_d(\log)/V_g</math>, threshold vs Length</li><li>➤ 3D fabrication process simulator with cross sectional viewer, facility to select different layers for visualization.</li><li>➤ Visualization of contacts and metallization created</li><li>➤ Checking of the self-aligned diffusion after the polysilicon gate is fabricated</li><li>➤ Check planes of VDD, VSS, and others signals</li><li>➤ Check the oxide structure, the low dielectric (Low K) and high K (<math>SiO_2</math>) sandwich, and passivation</li><li>➤ User can check the gate oxide and the MOS lateral drain diffusion structure</li><li>➤ Simulation of non-volatile memories such as EPROM, EEPROM and FLASH using double-gate MOS</li><li>➤ Erasure of floating gates and removal all electrons.</li><li>➤ Full length tutorial on MOS models is provided in manual, with details on all parameters</li><li>➤ Supports 1,3 and BSIM4 MOS models</li><li>➤ 200-pages documentation including several aspects of logic design</li><li>➤ More than 200 basic circuits ready to simulate</li></ul>
--	--	---



**FORMAT FOR QUOTATION SUBMISSION**

(In letterhead of the supplier with seal)

Date: \_\_\_\_\_

To:

\_\_\_\_\_  
\_\_\_\_\_

Sl. No.	Description of goods (with full Specifications)	Qty.	Unit	Quoted Unit rate in Rs. (Including Ex Factory price, excise duty, packing and forwarding, transportation, insurance, other local costs incidental to delivery and warranty/ guaranty commitments)	Total Price (A)	Sales tax and other taxes payable	
						In %	In figures (B)
<b>Total Cost</b>							

Gross Total Cost (A+B): Rs. \_\_\_\_\_

We agree to supply the above goods in accordance with the technical specifications for a total contract price of Rs. \_\_\_\_\_ (Amount in figures) (Rupees \_\_\_\_\_ amount in words) within the period specified in the Invitation for Quotations.



We confirm that the normal commercial warranty/ guarantee of \_\_\_\_\_ months shall apply to the offered items and we also confirm to agree with terms and conditions as mentioned in the Invitation Letter.

We hereby certify that we have taken steps to ensure that no person acting for us or on our behalf will engage in bribery.

Signature of Supplier

Name: \_\_\_\_\_

Address: \_\_\_\_\_

Contact No: \_\_\_\_\_