Shivaji University, Kolhapur

Department of Technology

Package Code	Package Name	Items	Description of Works/Goods	Qty	Method of Procurement
TEQIP-II/MH/MH1G05/114	Xilinx	Vertex 6 ML 605	"FPGA: XC6VLX240T-1FFG1156, Clocking: 200 MHz Oscillator (Differential) ,66 MHz Socketed Oscillator (Single-Ended) , SMA Connectors for external clock (Differential)"	1	Direct Contract
		Anvyl Spartan 6	6,822 slices, each containing four input LUTs and eight flip-flops ??2.1Mbits of fast block RAM ??four clock tiles (eight DCMs & four PLLs) ?58 DSP slices, ?500MHz+ clock speeds ??Spartan6-LX45 FPGA (XC6SLX45-CSG484-3) ??128MB DDR2 SDRAM, ? ?2MB SRAM"	1	
		Xilinx Vivado System Edition	IP and system centric design environment, system to IC level tools, AxI4 interconnect, IP-XACT packaging metadata, tool command language, synthesis verification tools	1	