B. Tech Electronics & Telecommunication Engineering

Summary of training on Verilog and VHDL programming

Online training session of 24 hours duration is organized for students of T.Y. B. Tech Electronics & Telecommunication Engineering program. In this add-on course students will learn Verilog and VHDL programming languages. Resource person is Mr. Tejeshwar Thorawade, Ph.D. Scholar, IIT Bombay and former Design and verification engineer at Samsung Inc.

The first session started on Saturday , 5th March 2023. On every Saturday the training session will be conducted between 11:00 am to 01:00 pm.

Resource person CV is as given below.

TEJESHWAR BHAGATSING THORAWADE

214076001@iitb.ac.in ; tejaswhar27@gmail.com | +91 7755992131

Research Interests

- Computer Architecture, Memory Architecture

Education

Indian Institute of Technology Bombay — Jul '21 – Present
CADSL, Department of Electrical Engineering — *Mumbai, India*
- Pursuing PhD in Electrical Engineering under Prof. Virendra Singh

Indian Institute of Technology Bombay — Jul '14 – May '18
Department of Electrical Engineering — *Mumbai, India*
- B.Tech. in Electrical Engineering with Hons. and with Minor in Systems and Control Eng. (CPI 8.12/10)

Academic Accolades

- Secured All India Rank 437 (44 in OBC category) in Joint Entrance Advanced Exam, 2014
- Awarded Kishore Vaigyanik Protsahan Yojana Fellowship, 2013 for securing 379th All India Rank
- Awarded the National Merit-Cum-Means Scholarship by the Government of India (2011-13)

Professional Experience

Chip Design Verification Engineer — Jul '18 – Jul '21
Samsung Semiconductor India R & D — *Bangalore, India*
- Part of Digital Television design verification team. Responsible for SoC verification of the HDMI block
- Developed a vendor agnostic UVM based test bench supporting 2 VIPs for verification of HDMI block
- Developed a UVM based test bench for IP verification of YC_BC_R 4:2:0 to YC_BC_R 4:4:4 converter IP
- Built expertise in HDMI 1.4, HDMI 2.0 and HDMI 2.1 protocol specifications

Intern — May '17 – Jul '17
YOLO Health — *Pune, India*
- Designed a 12 lead ECG module using ADS1298 and Atmega328p to send the data via Bluetooth to master controller for further processing and display

Research Experience

Consensus & Control in Multi-agent System — Aug '17 – May '18
Guide: Prof. Debasattam Pal — *Undergraduate Thesis*
- Worked on identifying leader for consensus in multi-agent dynamical system to optimize time and energy
- Ran simulations on MATLAB to study behaviour of leader-following multi-agent system in path topology
- Identified uncontrollable leader nodes in a path graph by using MATLAB and studied the results
- Proposed and proved a theorem to identify uncontrollable leader nodes in a path graph

Academic Projects

Processor Architecture — Jul '16 – Nov '16
Guide: Prof. Virendra Singh — *Course Project*
- Designed, optimized and implemented multi-cycle, 8-register, 16-bit computer processor on FPGA
- Designed a 6 stage pipelined processor; 8-register, 16-bit computer processor using VHDL as HDL

IIT Bombay Racing
Guide: Prof. Amber Shrivastava
A student-team which designs and manufactures electric car for participation in Formula Student, UK

Chief Electrical Officer — Jul '17 – Jul '18
- Head of the Electronic Control Unit, Data Acquisition and System Integration subsystems
- Spearheaded team for testing, debugging, fine tuning of the car and post processing data

Design Engineer — Aug '16 – Apr '17
- Responsible for design and fabrication of Electronic Control Unit and System integration subsystems

Junior Design Engineer — Aug '15 – Jul '16
- Worked on Electronic Differential sub-sytem to design and implement torque vectoring

Technical Skills

Languages: VHDL, UVM, System Verilog, Verilog, C++, Python, Perl
Softwares: Quartus Prime Lite, GHDL, Modelsim, iverilog, GTKWave, Simvision, Verdi, MATLAB, Eagle